February 2006

FAIRCHILD SEMICONDUCTOR®

FDM2509NZ

Monolithic Common Drain N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

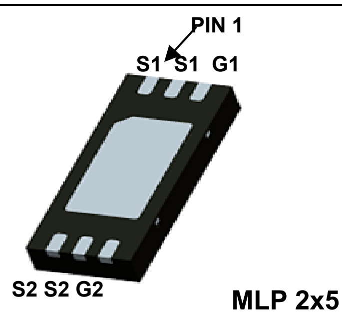
This dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $R_{DS(ON)}$ @ V_{GS} = 2.5v on special MicroFET lead frame with all the drains on one side of the package.

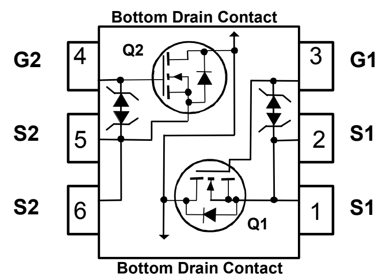
Applications

- Li-Ion Battery Pack

Features

- 8.7 A, 20 V $R_{DS(ON)}$ = 18 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 24 mΩ @ V_{GS} = 2.5 V
- ESD protection diode (note 3)
- Low Profile – 0.8mm maximum – in the new package MicroFET 2x5 mm





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current – Continuous	(Note 1a)	8.7	A
	– Pulsed		30	
P_D	Power Dissipation (Steady State)	(Note 1a)	2.2	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	55	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Drain)		2	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2509Z	FDM2509NZ	7''	12mm	3000 units

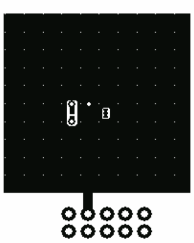
Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate–Body Leakage,	V_{GS} = ±12 V, V_{DS} = 0 V			±10	μA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250 μA	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25□C		–3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 8.7 A V_{GS} = 4.0 V, I_D = 8.5 A V_{GS} = 3.1 V, I_D = 8.1 A V_{GS} = 2.5 V, I_D = 7.6 A V_{GS} = 4.5 V, I_D = 8.7 A, T_J = 125°C		13 13.5 15.5 18 18.4	18 19 21 24 25	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 8.7 A		36		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		1200		pF
C_{oss}	Output Capacitance			320		pF
C_{rss}	Reverse Transfer Capacitance			185		pF
R_G	Gate Resistance	V_{GS} = 50mV, f = 1.0 MHz		2		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn–On Rise Time			15	27	ns
$t_{d(off)}$	Turn–Off Delay Time			27	43	ns
t_f	Turn–Off Fall Time			12	22	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 8.7 A, V_{GS} = 4.5 V		12	17	nC
Q_{gs}	Gate–Source Charge			2		nC
Q_{gd}	Gate–Drain Charge			4		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.8	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.8 A (Note 2)		0.7	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 8.7 A, dI_F/dt = 100 A/μs		20		nS
Q_{rr}	Diode Reverse Recovery Charge			6.4		nC

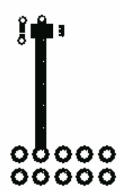
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 55°C/W when mounted on a 1in^2 pad of 2 oz copper

Scale 1 : 1 on letter size paper



b) 145°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%
3. The diode connected between the gate and the source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

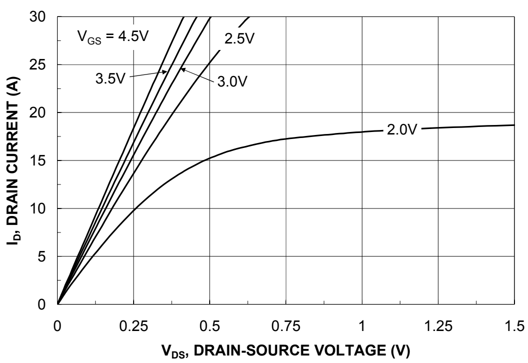


Figure 1. On-Region Characteristics.

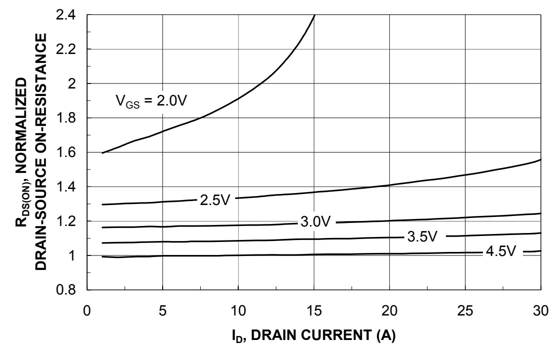


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

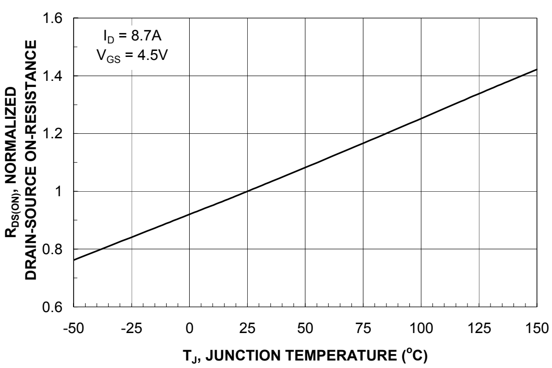


Figure 3. On-Resistance Variation with Temperature.

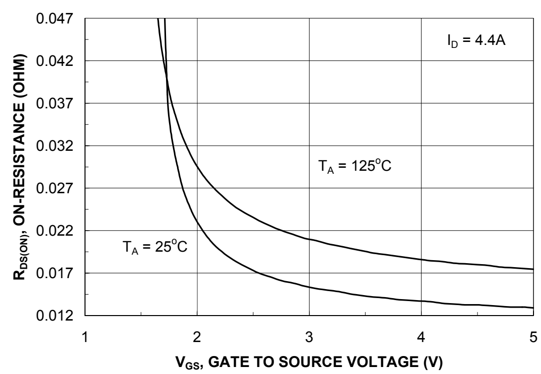


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

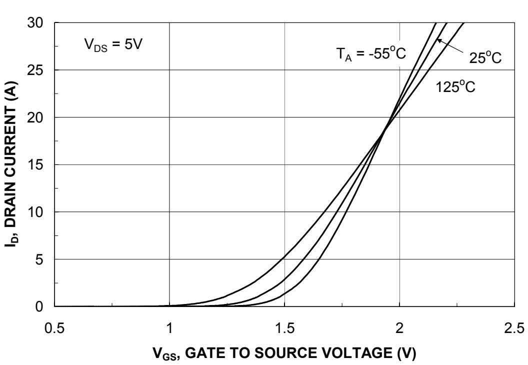


Figure 5. Transfer Characteristics.

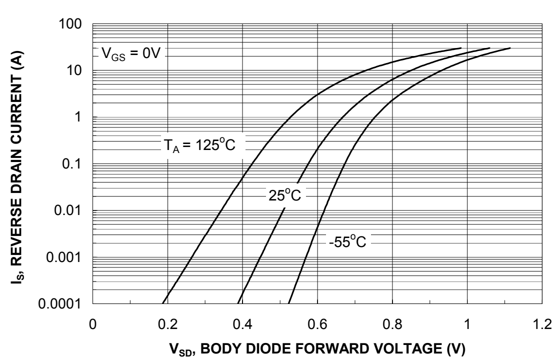


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

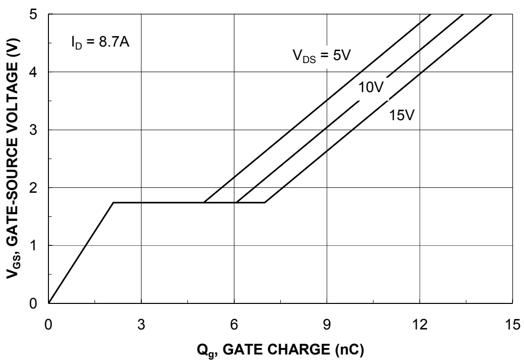


Figure 7. Gate Charge Characteristics.

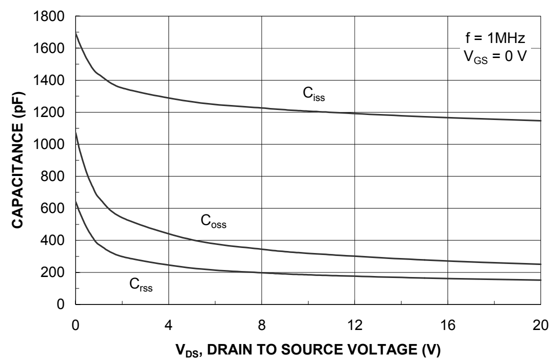


Figure 8. Capacitance Characteristics.

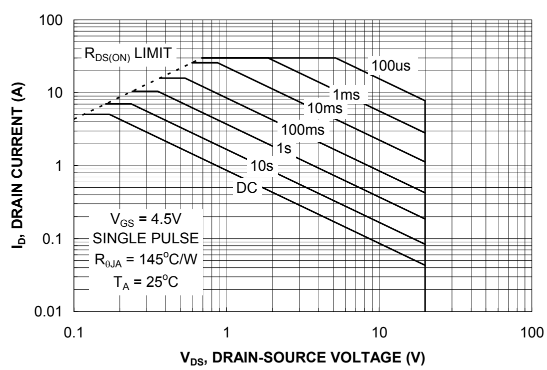


Figure 9. Maximum Safe Operating Area.

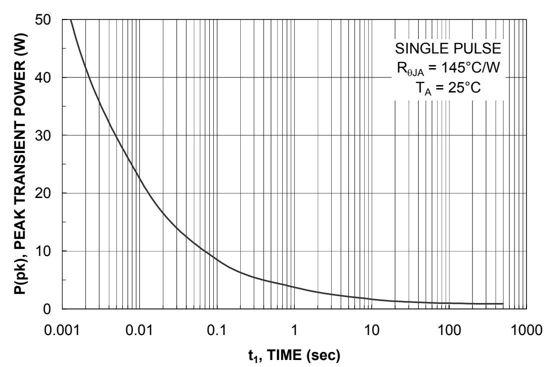


Figure 10. Single Pulse Maximum Power Dissipation.

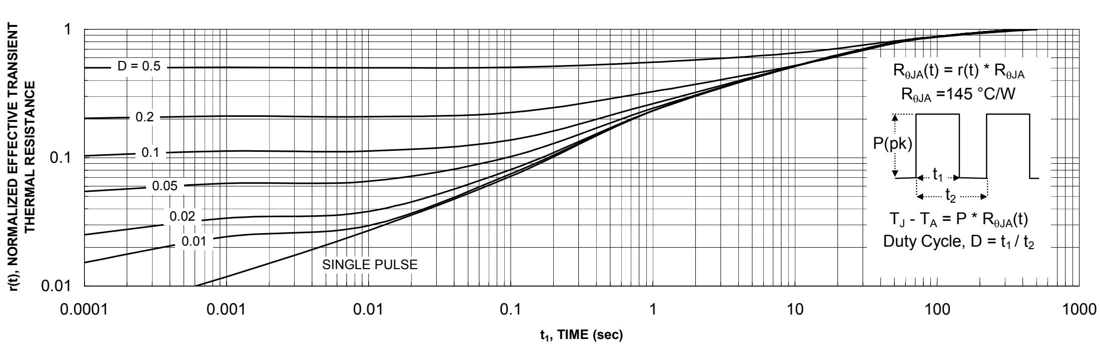
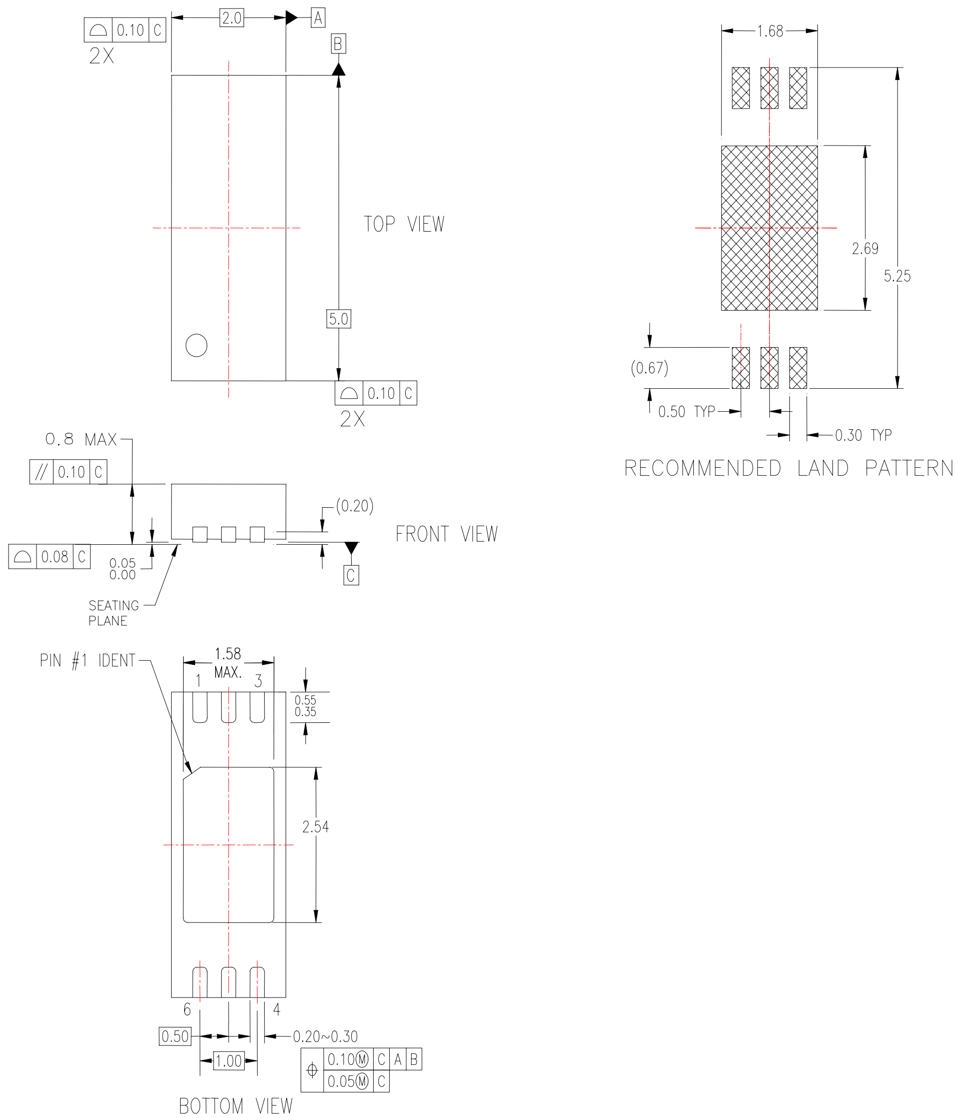


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES:

A. NON-STANDARD JEDEC REGISTERED MOLDED PACKAGE OUTLINE.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP06XrevA

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